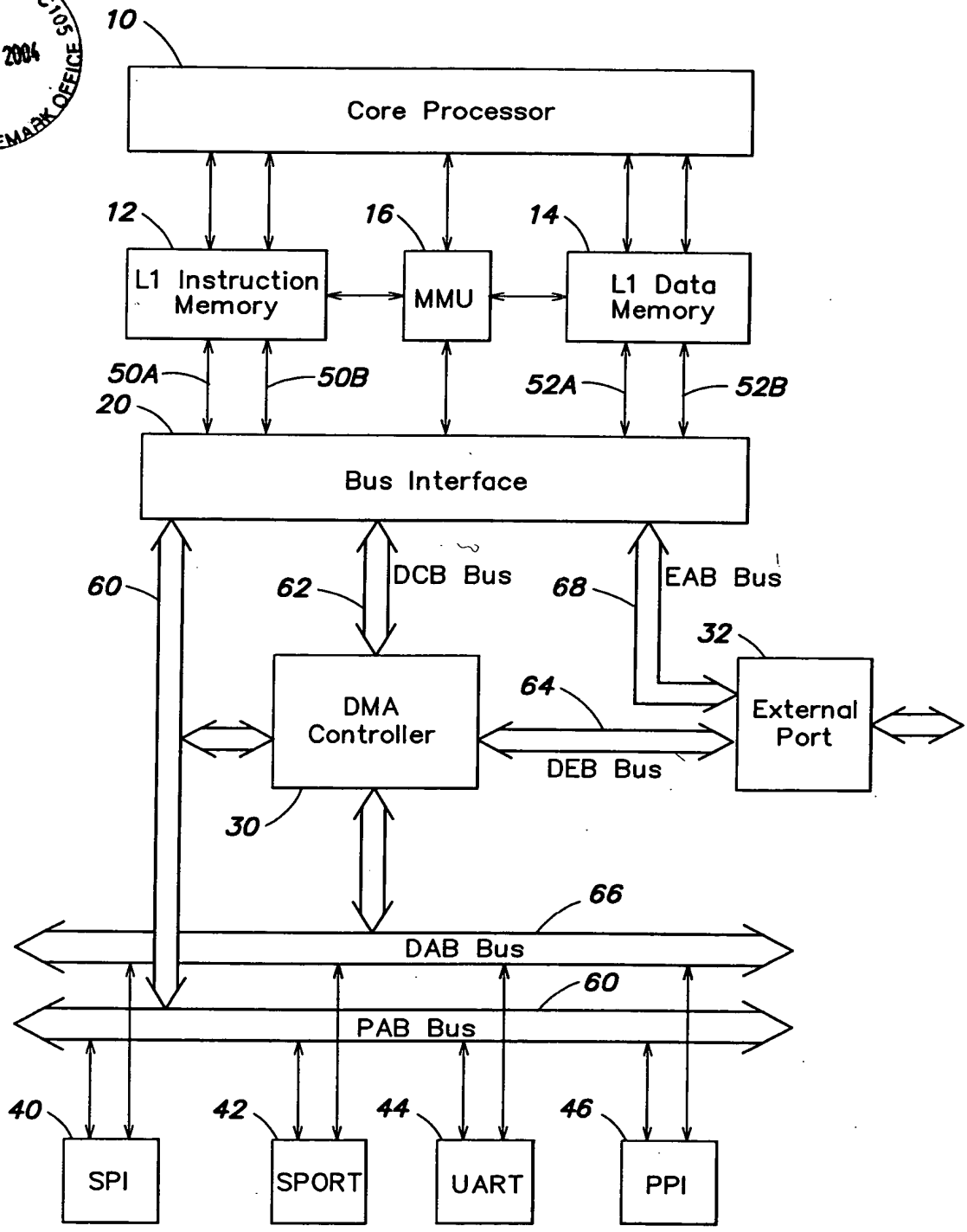

FIG. 1

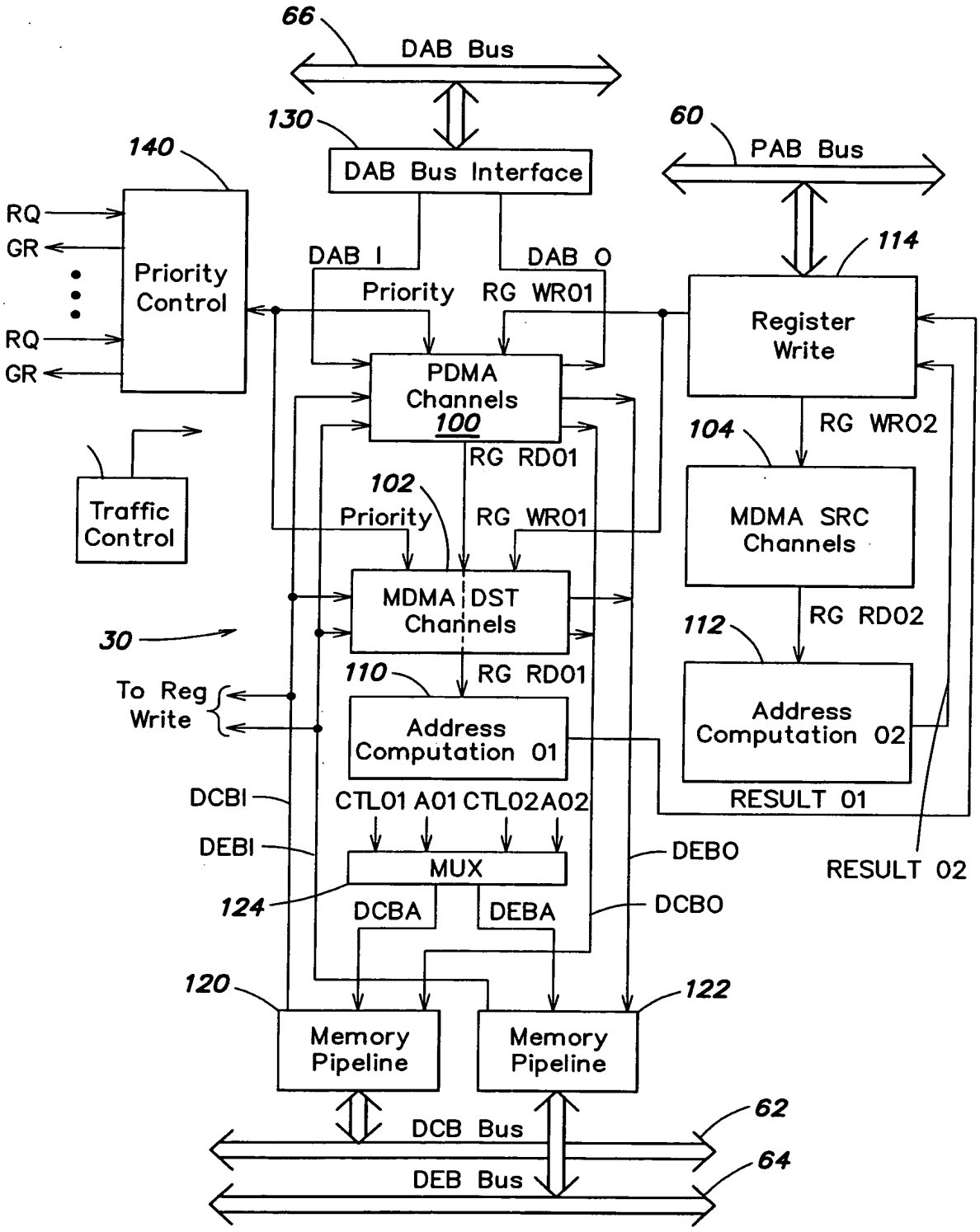
66
DAB Bus
130
DAB Bus Interface
60
PAB Bus
140
RQ
GR
RQ
GR
Priority Control
DAB I
DAB O
Priority
RG WR01
114
Register Write
PDMA Channels
100
RG RD01
104
RG WR02
Traffic Control
102
Priority
RG WR01
MDMA SRC Channels
MDMA DST Channels
RG RD02
30
112
To Reg Write
110
RG RD01
Address Computation 01
Address Computation 02
DCBI
CTL01 A01 CTL02A02
RESULT 01
DEBI
MUX
DEBO
RESULT 02
124
DCBA
DEBA
DCBO
120
122
Memory Pipeline
Memory Pipeline
62
DCB Bus
64
DEB Bus

FIG. 2

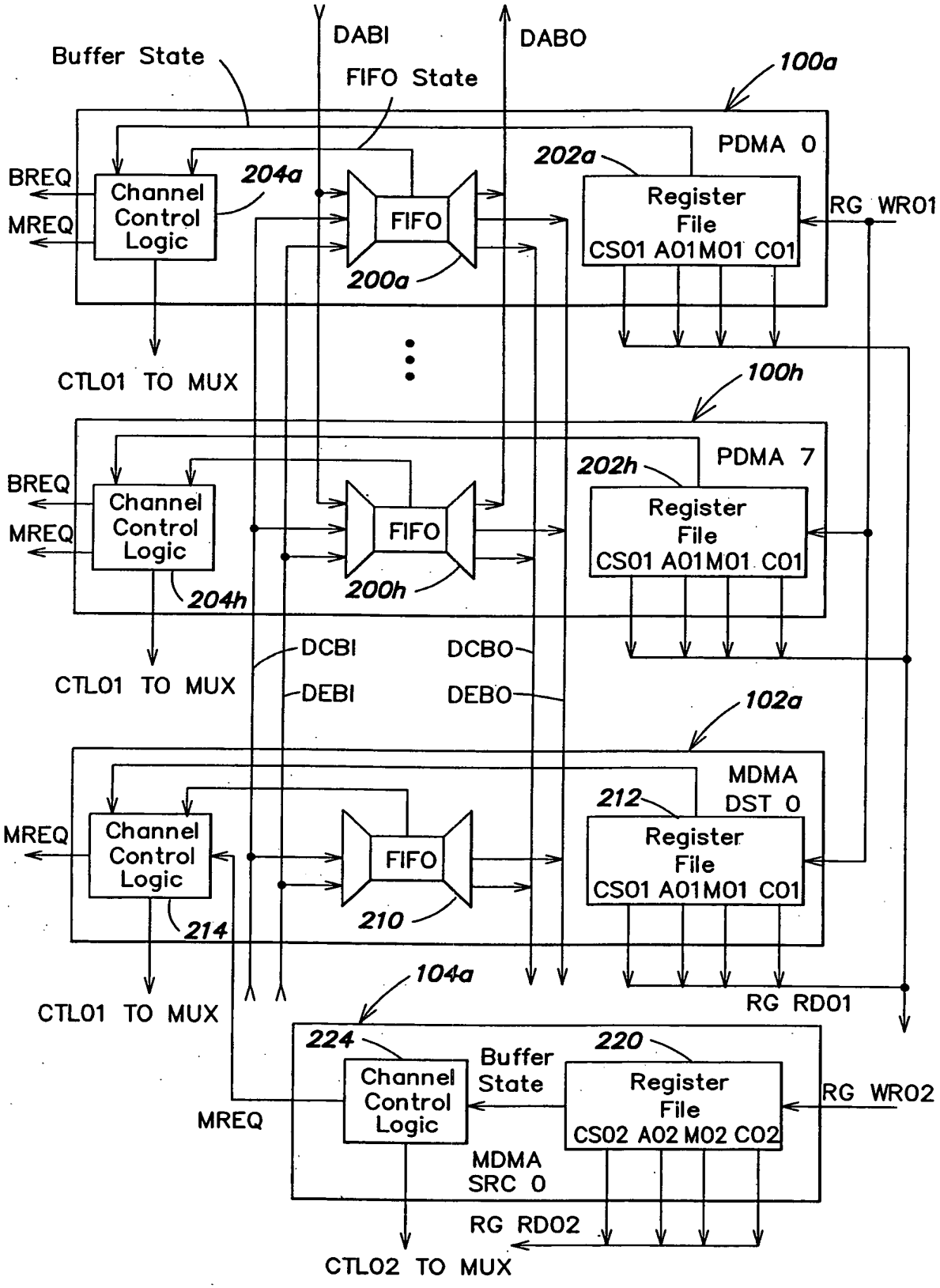
DABI
DABO
Buffer State
FIFO State
100a
PDMA 0
202a
BREQ
MREQ
Channel Control Logic
204a
FIFO
200a
Register File
CS01 A01 M01 C01
RG WR01
CTL01 TO MUX
100h
PDMA 7
202h
BREQ
MREQ
Channel Control Logic
204h
FIFO
200h
Register File
CS01 A01 M01 C01
DCBI
DCBO
DEBI
DEBO
CTL01 TO MUX
102a
MDMA DST 0
212
MREQ
Channel Control Logic
214
FIFO
210
Register File
CS01 A01 M01 C01
CTL01 TO MUX
104a
RG RD01
224
220
Buffer State
Channel Control Logic
Register File
CS02 A02 M02 C02
RG WR02
MREQ
MDMA SRC 0
RG RD02
CTL02 TO MUX

FIG. 3

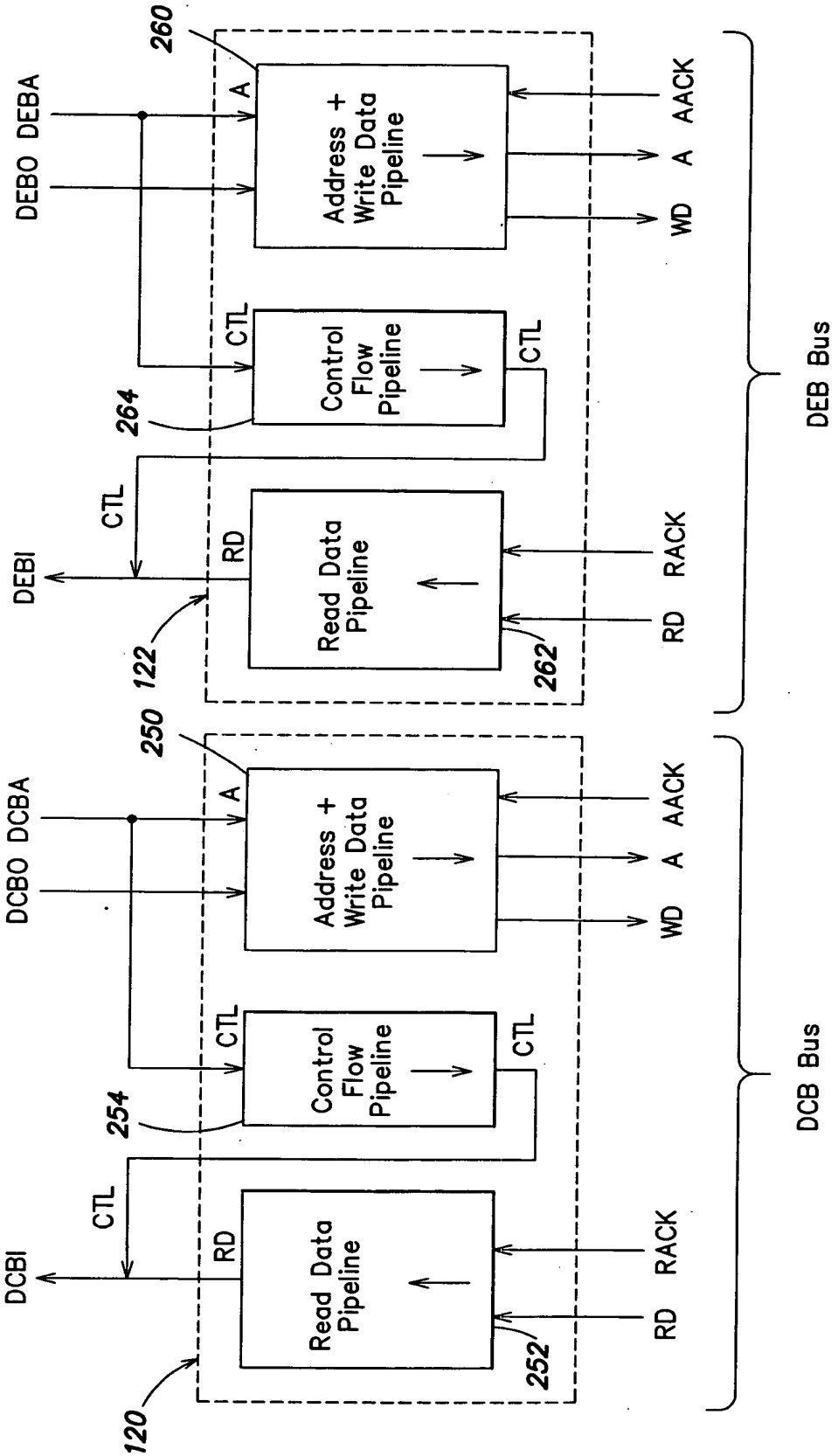
260
DEBO DEBA
A
Address + Write Data Pipeline
WD A AACK
CTL
Control Flow Pipeline
CTL
264
CTL
DEBI
RD
Read Data Pipeline
RD RACK
122
262
DEB Bus
250
DCBO DCBA
A
Address + Write Data Pipeline
WD A AACK
CTL
Control Flow Pipeline
CTL
254
CTL
DCBI
RD
Read Data Pipeline
RD RACK
120
252
DCB Bus

FIG. 4

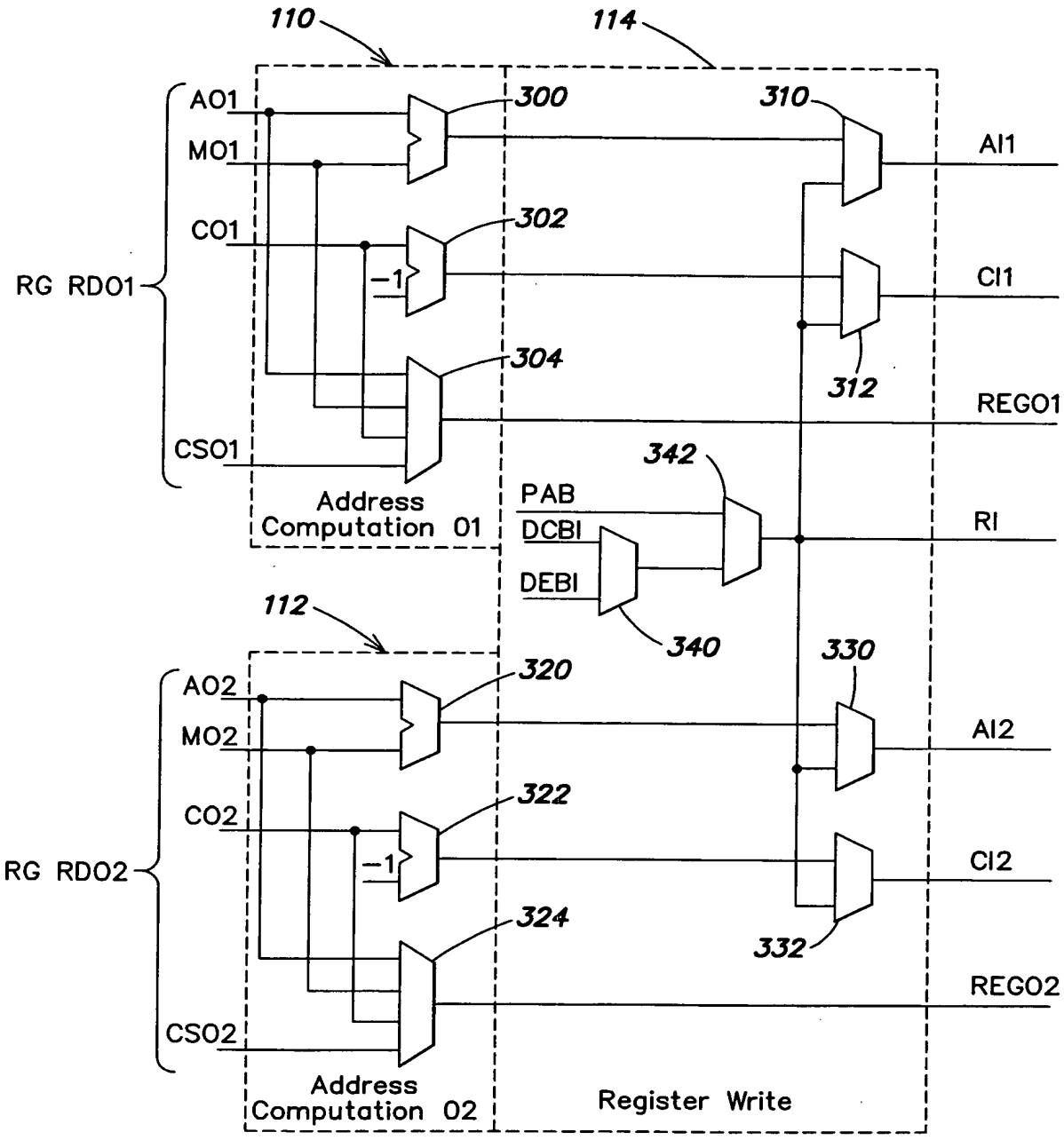
110
114
AO1
MO1
CO1
RG RDO1
CSO1
300
302
304
-1
310
AI1
CI1
312
REGO1
342
PAB
DCBI
DEBI
340
RI
Address
Computation 01
112
AO2
MO2
CO2
RG RDO2
CSO2
320
322
324
-1
330
AI2
CI2
332
REGO2
Address
Computation 02
Register Write

FIG. 5

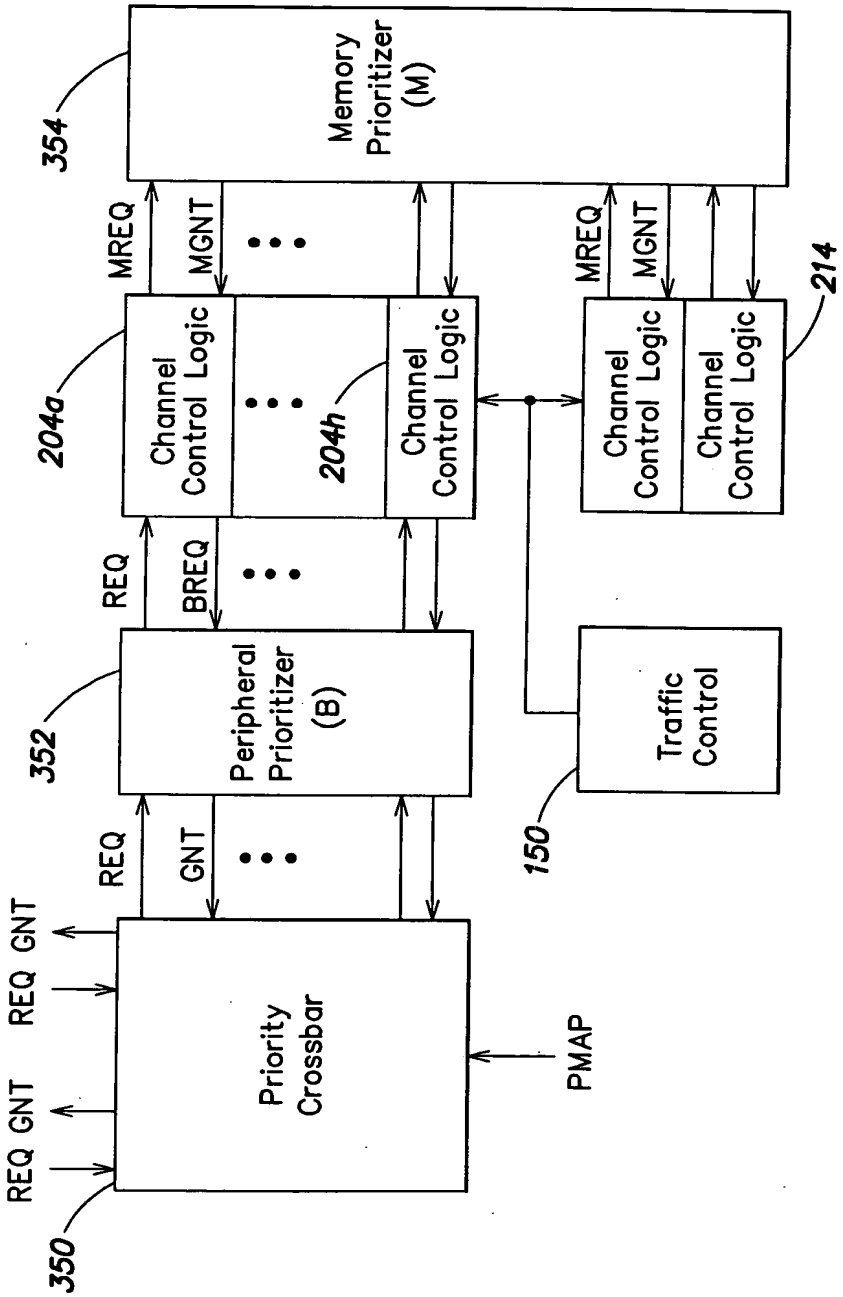
Memory Prioritizer (M)
354
MREQ
MGNT
MREQ
MGNT
214
204a
Channel Control Logic
204h
Channel Control Logic
Channel Control Logic
Channel Control Logic
REQ
BREQ
352
Peripheral Prioritizer (B)
Traffic Control
150
REQ
GNT
REQ GNT
REQ GNT
Priority Crossbar
PMAP
350

FIG. 6

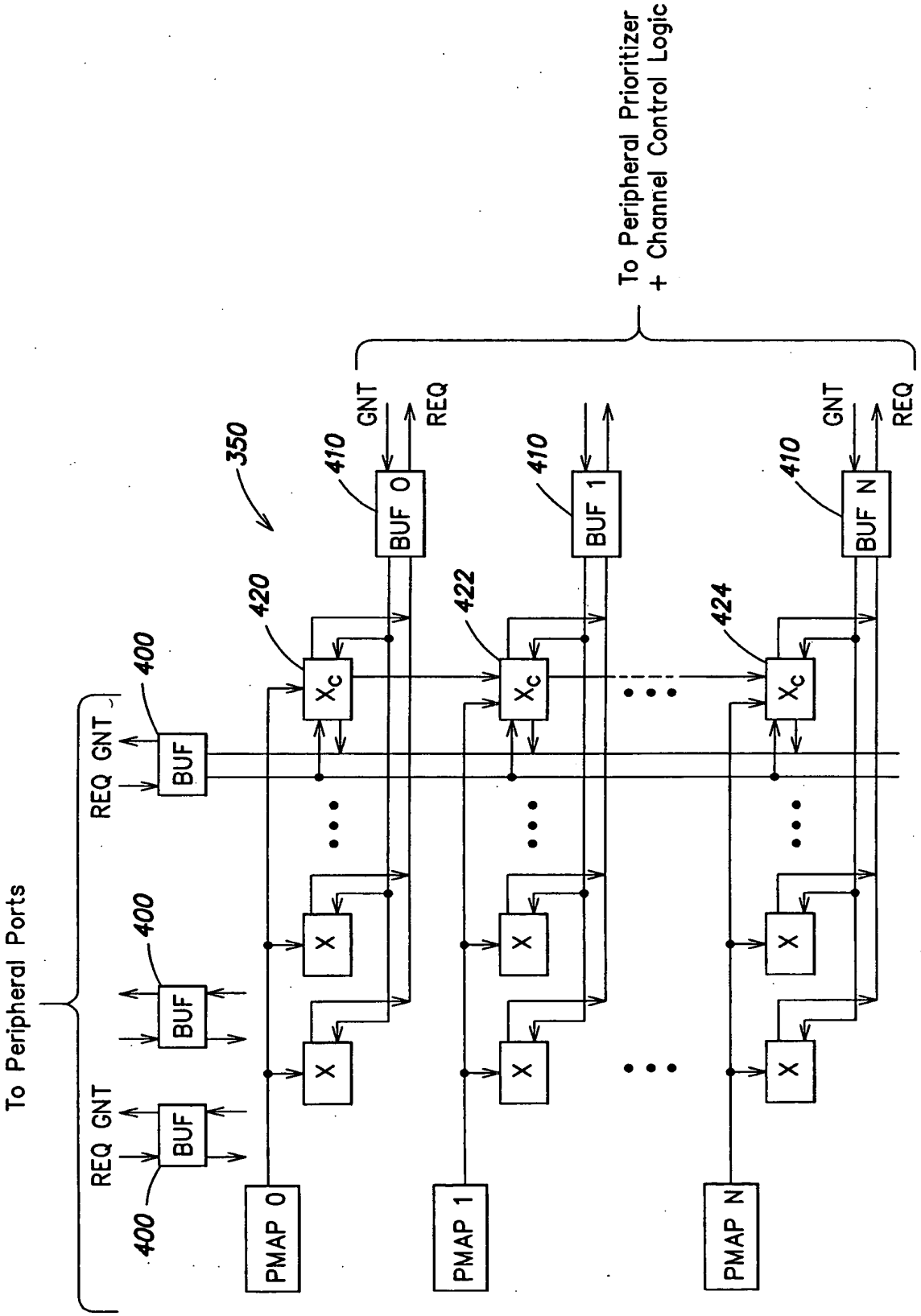
To Peripheral Prioritizer
+ Channel Control Logic
To Peripheral Ports
REQ GNT
REQ GNT
350
410
410
410
GNT
REQ
GNT
REQ
BUF 0
BUF 1
BUF N
420
422
424
400
400
400
BUF
BUF
BUF
Xc
Xc
Xc
X
X
X
X
X
X
PMAP 0
PMAP 1
PMAP N

FIG. 7A

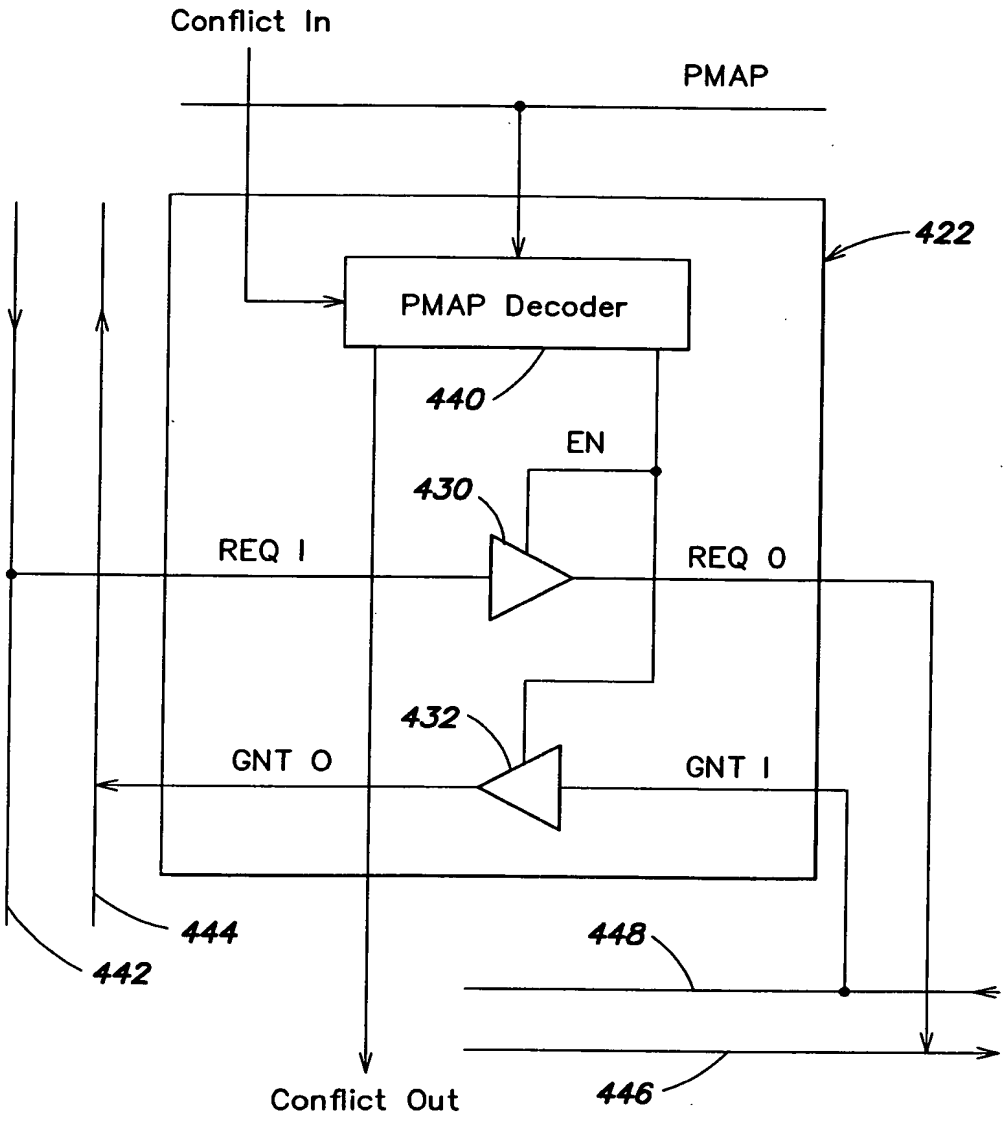
Conflict In
PMAP
422
PMAP Decoder
440
EN
430
REQ I
REQ O
432
GNT O
GNT I
444
442
448
446
Conflict Out

FIG. 7B

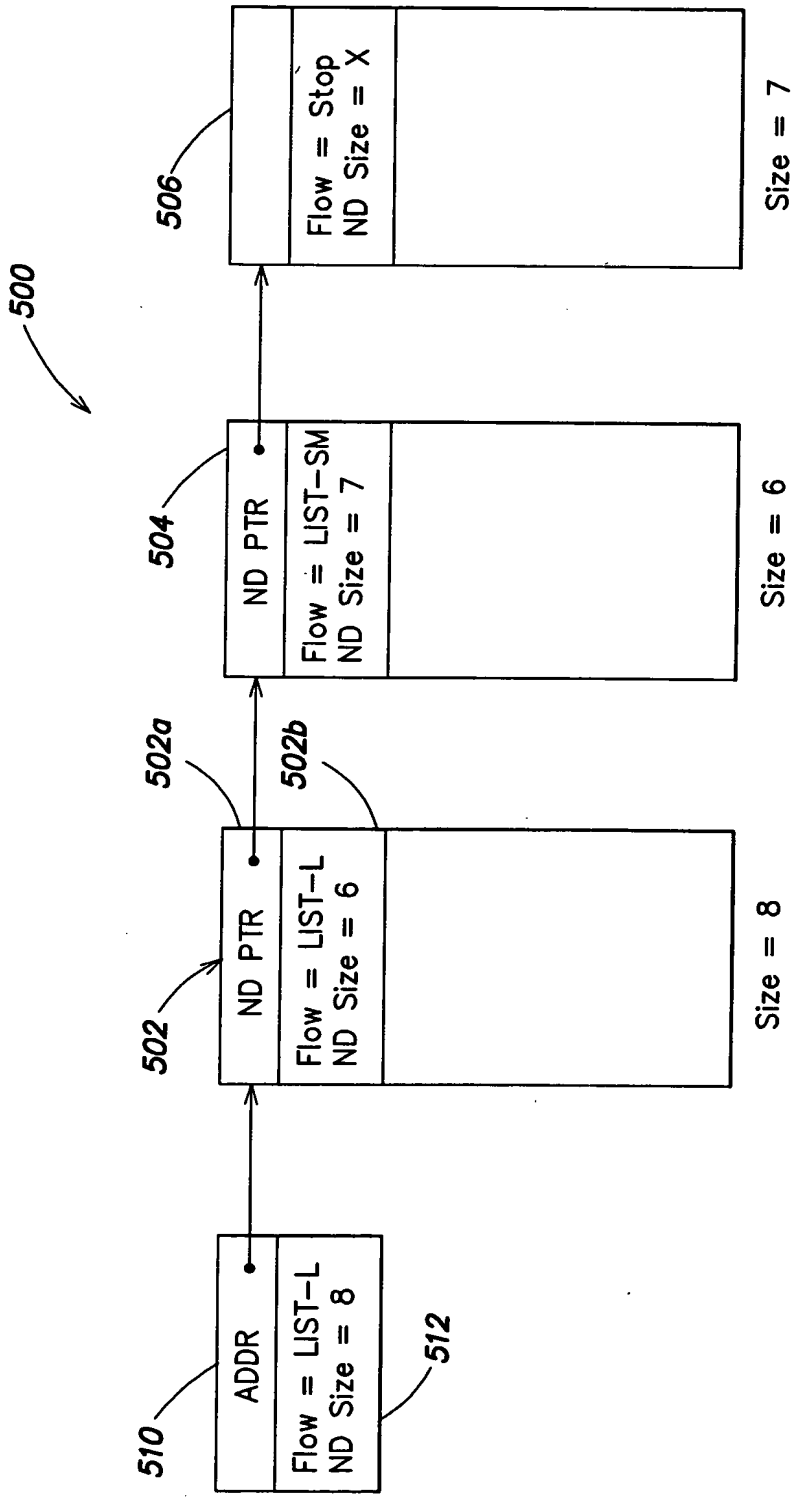
500
506
Flow = Stop
ND Size = X
Size = 7
504
ND PTR
Flow = LIST-SM
ND Size = 7
Size = 6
502a
502b
502
ND PTR
Flow = LIST-L
ND Size = 6
Size = 8
510
ADDR
Flow = LIST-L
ND Size = 8
512

FIG. 8

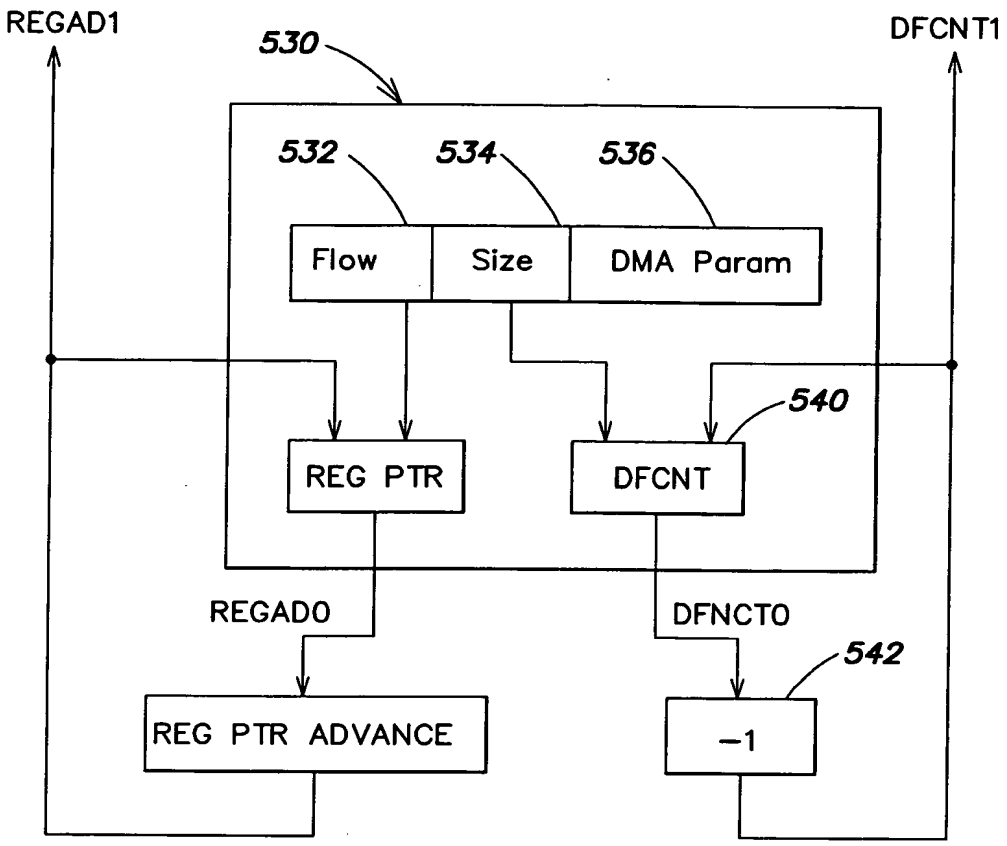
REGAD1
530
DFCNT1
532
534
536
Flow
Size
DMA Param
540
REG PTR
DFCNT
REGAD0
DFNCT0
542
REG PTR ADVANCE
−1

FIG. 9

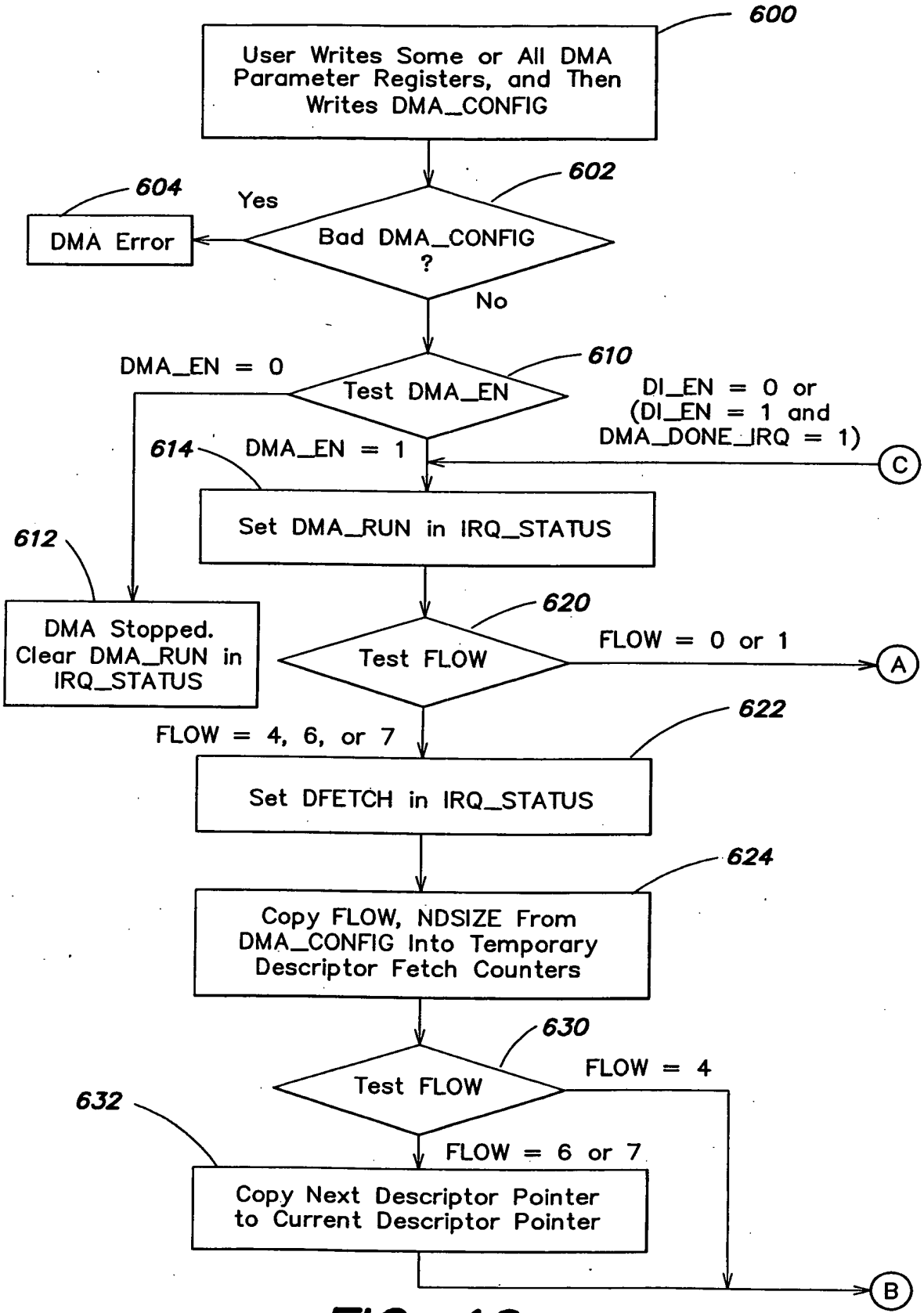
600
User Writes Some or All DMA Parameter Registers, and Then Writes DMA_CONFIG
602
Bad DMA_CONFIG ?
Yes
604
DMA Error
No
610
Test DMA_EN
DMA_EN = 0
DI_EN = 0 or (DI_EN = 1 and DMA_DONE_IRQ = 1)
C
614
DMA_EN = 1
Set DMA_RUN in IRQ_STATUS
612
DMA Stopped. Clear DMA_RUN in IRQ_STATUS
620
Test FLOW
FLOW = 0 or 1
A
622
FLOW = 4, 6, or 7
Set DFETCH in IRQ_STATUS
624
Copy FLOW, NDSIZE From DMA_CONFIG Into Temporary Descriptor Fetch Counters
630
Test FLOW
FLOW = 4
632
FLOW = 6 or 7
Copy Next Descriptor Pointer to Current Descriptor Pointer
B

FIG. 10

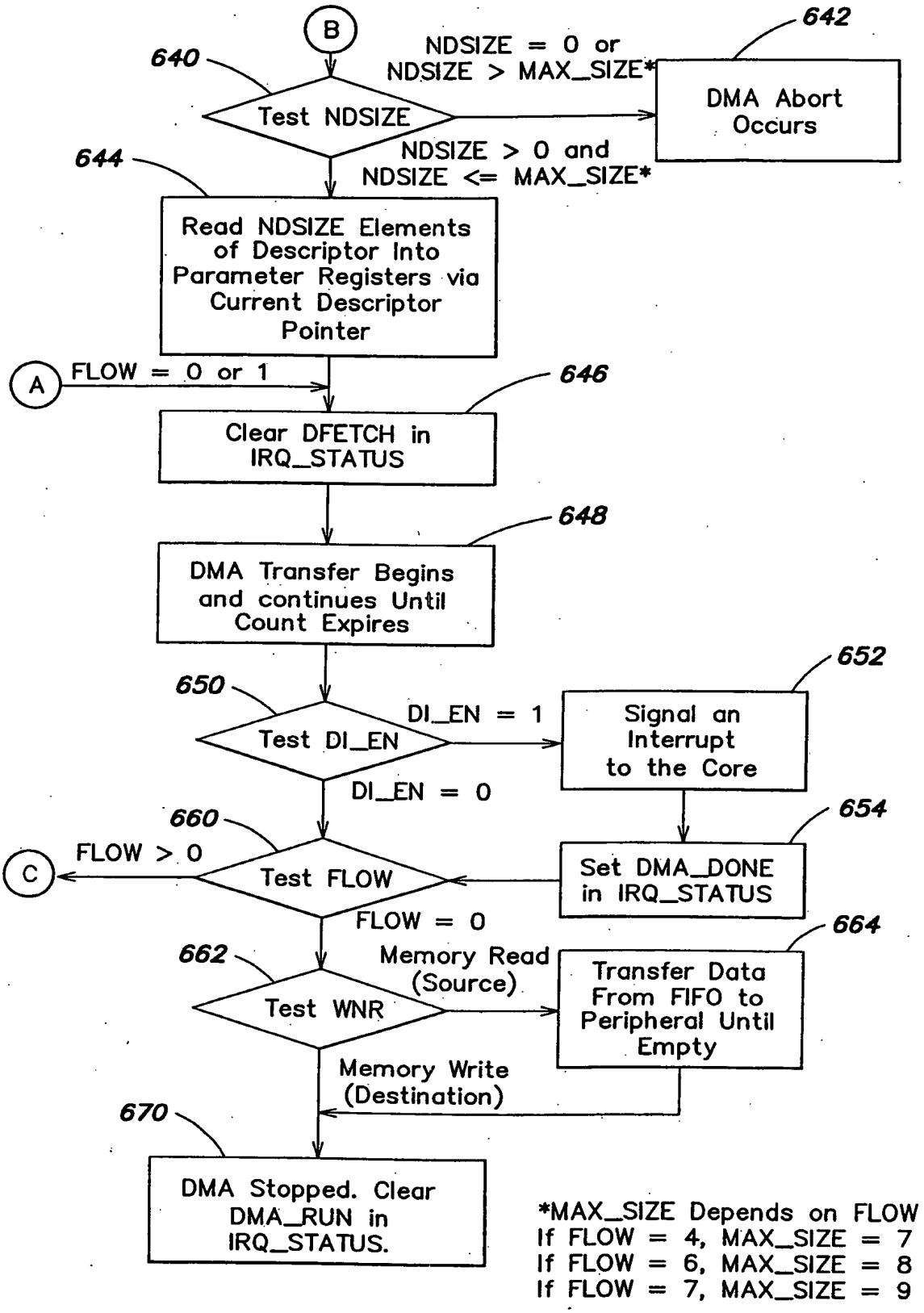
B
640
Test NDSIZE
NDSIZE = 0 or
NDSIZE > MAX_SIZE*
642
DMA Abort
Occurs
NDSIZE > 0 and
NDSIZE <= MAX_SIZE*
644
Read NDSIZE Elements
of Descriptor Into
Parameter Registers via
Current Descriptor
Pointer
A
FLOW = 0 or 1
646
Clear DFETCH in
IRQ_STATUS
648
DMA Transfer Begins
and continues Until
Count Expires
650
Test DI_EN
DI_EN = 1
652
Signal an
Interrupt
to the Core
DI_EN = 0
660
Test FLOW
C
FLOW > 0
654
Set DMA_DONE
in IRQ_STATUS
FLOW = 0
662
Test WNR
Memory Read
(Source)
664
Transfer Data
From FIFO to
Peripheral Until
Empty
Memory Write
(Destination)
670
DMA Stopped. Clear
DMA_RUN in
IRQ_STATUS.
*MAX_SIZE Depends on FLOW
If FLOW = 4, MAX_SIZE = 7
If FLOW = 6, MAX_SIZE = 8
If FLOW = 7, MAX_SIZE = 9

FIG. 11